UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/042,812	01/09/2002	Cheng-Lien Chiang	BDG005	7608

7590 08/15/2003

David M. Sigmond
2440 Andrew Drive
Superior, CO 80027

EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 08/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/042,812	CHIANG, CHENG-LIEN	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 120* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 120* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *08 May 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on May 8, 2003 has been received and entered in the case.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the following limitation in claim 96 "the first distance is about twice the second distance" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect may be deferred until after the examiner has considered the proposed drawing correction. Failure to timely submit the proposed drawing correction will result in the abandonment of the application.

Specification

4. The disclosure is objected to because of the following informalities:

On page 8, the specification needs a brief description of the drawings for Figs. 1A ~ 15B.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 ~ 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin et al. in view of Nakamura et al.

Regarding claim 1, Shin et al. discloses in Fig. 1A, Fig. 1B, Fig. 10B and column 6, lines 36 ~ 40 a semiconductor package device, comprising:

- an insulative housing (40) with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces;
- a semiconductor chip (20) within the insulative housing, wherein the chip includes an upper surface and a lower surface, and the upper surface includes a conductive pad (31);

- a terminal (4 and 4') that protrudes downwardly from and extends through the bottom surface and is electrically connected to the pad; and
- a lead (2) that protrudes laterally from and extends through the side surface and is electrically connected to the pad,
- wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

Shin et al. does not disclose the insulative housing including a first single-piece housing portion and a second single-piece housing portion and the first single-piece housing portion contacting the lead and being spaced from the terminal, the second single-piece housing portion contacting the first single-piece housing portion and the terminal. However, Nakamura et al. teaches in Fig. 1 an insulative housing (7 and 8) including a first single-piece housing portion (7) and a second single-piece housing portion (8) and the first single-piece housing portion (7) contacting a lead (2) and being spaced from a terminal (4), the second single-piece housing portion (8) contacting the first single-piece housing portion and the terminal. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Shin et al. by using the first and second single-piece housing portion for the insulative housing as taught by Nakamura et al. The ordinary artisan would have been motivated to modify Shin et al. in the manner described above for at least the purpose of providing a firm electrical connection with a circuit conductor layer formed on a substrate in a semiconductor device (column 5, lines 55 ~ 57).

Regarding claim 2, Nakamura et al. discloses in Fig. 1 and Fig. 5 the first single-piece housing portion (27) providing the top surface, the side surface and a peripheral portion of the bottom surface, and the second single-piece housing portion (28) providing a central portion of the bottom surface within the peripheral portion of the bottom surface.

Regarding claim 3, Nakamura et al. discloses in Fig. 1 and Fig. 5 the first single-piece housing portion contacting the lower surface.

Regarding claim 4, Nakamura et al. discloses in Fig. 1 the insulative housing consisting of the first and second single-piece housing portions.

Regarding claim 5, Shin et al. disclóses in Fig. 1A, Fig. 1B, Fig. 10B and column 6, lines 36 ~ 40 the terminal being the only electrical conductor that extends through the top or bottom surfaces and being electrically connected to the pad.

Regarding claim 6, Shin et al. discloses in Fig. 1A, Fig. 1B, Fig. 10B and column 6, lines 36 ~ 40 the terminal being a plated metal. Further, the limitation "plated metal" is a product-by-process claim language. Even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186**

USPQ 116; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claims 7 and 17, Shin et al. discloses in Fig. 1A, Fig. 1B and Fig. 10B the terminal being within a periphery of the chip, and the lead being outside the periphery of the chip.

Regarding claim 8, Shin et al. discloses in Fig. 1A, Fig. 1B and Fig. 10B the device being devoid of an electrical conductor that extends through the top surface and being electrically connected to the pad.

Regarding claims 9 and 19, Shin et al. discloses in Fig. 1A, Fig. 10B and Fig. 14 the device including a plurality of terminals and leads, the chip including a plurality of pads, each of the terminals are electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through the side surface and an opposing peripheral side surface of the insulative housing.

Regarding claims 10 and 20, Shin et al. discloses in Fig. 1A, Fig. 1B and Fig. 10B the device being devoid of wire bonds, TAB leads and solder joints.

Regarding claim 11, Shin et al. discloses in Fig. 1A, Fig. 1B, Fig. 10B and column 6, lines 36 ~ 40 a semiconductor package device, comprising:

- an insulative housing (40) with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces;
- a semiconductor chip (20) within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, the upper surface includes a conductive pad (31), the upper surfaces faces towards the bottom surface and faces away from the top surface, and the insulative housing contacts the lower surface;
- a terminal (4 and 4') that protrudes downwardly from and extends through the bottom surface and is spaced from the side surface and is electrically connected to the pad; and
- a lead (2) that protrudes laterally from and extends through the side surface and is electrically connected to the pad,
- wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

Shin et al. does not disclose the insulative housing consisting of a first single-piece housing portion and a second single-piece housing portion and the first single-piece housing portion contacting the lower surface and the lead and being spaced from the terminal, the second single-piece housing portion contacting the first single-piece housing portion and the terminal. However, Nakamura et al. teaches in Fig. 1 an insulative housing (7 and 8) consisting of a first single-piece housing portion (7) and a second single-piece housing portion (8) and the first single-piece housing portion (7) contacting a lead (2) and being spaced from a terminal (4), the second single-piece housing portion (8)

contacting the first single-piece housing portion and the terminal. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Shin et al. by using the first and second single-piece housing portion for the insulative housing as taught by Nakamura et al. The ordinary artisan would have been motivated to modify Shin et al. in the manner described above for at least the purpose of providing a firm electrical connection with a circuit conductor layer formed on a substrate in a semiconductor device (column 5, lines 55 ~ 57).

Regarding claim 12, Nakamura et al. discloses in Fig. 1 the first single-piece housing portion being farther from the top surface than the lower surface is from the top surface.

Regarding claim 13, Nakamura et al. discloses in Fig. 1 and Fig. 5 the first single-piece housing portion providing the top surface, the side surface and a peripheral portion of the bottom surface, and the second single-piece housing portion providing a central portion of the bottom surface within the peripheral portion of the bottom surface.

Regarding claim 14, Shin et al. discloses in Fig. 1A, Fig. 1B and Fig. 10B the peripheral portion of the bottom surface being outside a periphery of the chip, and the central portion of the bottom surface being within and outside the periphery of the chip.

Regarding claim 15, Nakamura et al. discloses in Fig. 1, column 6, lines 49 ~ 55 and column 8, lines 53 ~ 58 the first single-piece housing portion being a transfer molded material, and the second single-piece housing portion being not a transfer molded material. Further, the limitation "transfer molded material" is a product-by-process claim language. Even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability

of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 16, Nakamura et al. discloses in Fig. 1 the second single-piece housing portion including first and second opposing surfaces, the first surface contacting the lead and the second surface providing a portion of the bottom surface.

Regarding claim 18, Shin et al. discloses in Fig. 10B and column 21, lines 22 ~ 28 the terminal being integral with a routing line that is plated on the lead inside the insulative housing, outside a periphery of the terminal and outside a periphery of the chip.

Regarding claim 21, Shin et al. discloses in Fig. 1A, Fig. 1B, Fig. 10B, Fig. 14 and column 6, lines 36 ~ 40 a semiconductor package device, comprising:

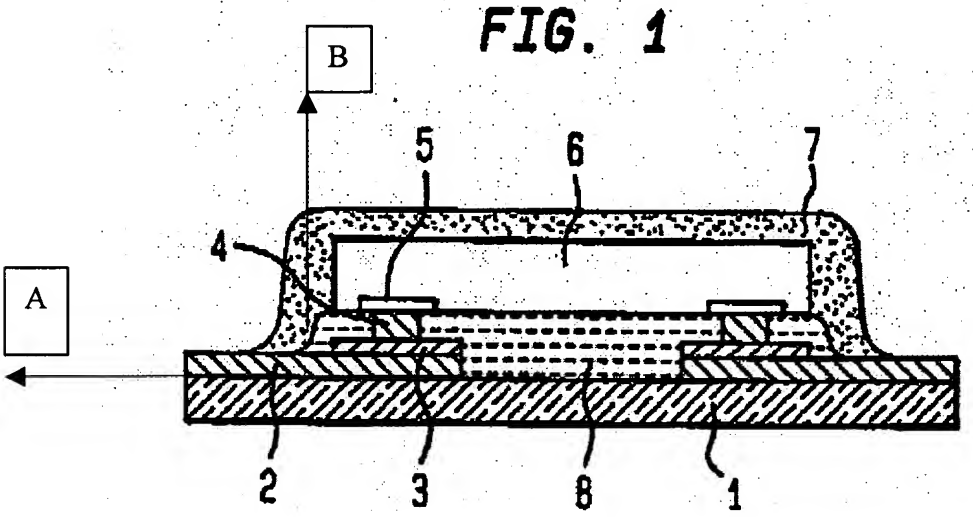
- an insulative housing (40) with a top surface, a bottom surface, and peripheral side surfaces between the top and bottom surfaces;

- a semiconductor chip (20) within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, and the upper surface includes a conductive pad;
- a terminal (4 and 4') that protrudes downwardly from and extends through a central portion of the bottom surface and is spaced from the side surfaces and is electrically connected to the pad; and
- a lead (2) that protrudes laterally from and extends through one of the side surfaces and is electrically connected to the pad,
- wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

Shin et al. does not disclose the bottom surface including a peripheral portion adjacent to the side surfaces and a central portion within the peripheral portion and spaced from the side surfaces, and the peripheral portion protrudes downwardly from the central portion. However, Nakamura et al. discloses in Fig. 1 a bottom surface (A) including a peripheral portion (B) adjacent to side surfaces and a central portion (area of 8) within the peripheral portion and spaced from the side surfaces, and the peripheral portion protruding downwardly from the central portion. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Shin et al. by using the peripheral portion as taught by Nakamura et al. The ordinary artisan would have been motivated to modify Shin et al. in the manner described above for at least the purpose of providing a firm electrical connection with a circuit

conductor layer formed on a substrate in a semiconductor device (column 5, lines 55 ~ 57).

FIG. 1



Regarding claims 22 and 32, Shin et al. discloses the claimed invention except for the insulative housing consisting of a first single-piece housing portion that contacts the lower surface and the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion and the terminal. However, Nakamura et al. discloses in Fig. 1 an insulative housing (7 and 8) consisting of a first single-piece housing portion (7) that contacts the lower surface and the lead (2) and is spaced from the terminal (4) and a second single-piece housing portion (8) that contacts the first single-piece housing portion and the terminal. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Shin et al. by using the first and second single-piece housing portion for

the insulative housing as taught by Nakamura et al. The ordinary artisan would have been motivated to further modify Shin et al. in the manner described above for at least the purpose of providing a firm electrical connection with a circuit conductor layer formed on a substrate in a semiconductor device (column 5, lines 55 ~ 57).

Regarding claims 23 and 33, Nakamura et al. discloses in Fig. 1 and Fig. 4 the first single-piece housing portion providing the top surface, the side surfaces and the peripheral portion of the bottom surface, and the second single-piece housing portion providing the central portion of the bottom surface.

Regarding claims 24 and 34, Nakamura et al. discloses in Fig. 1 the peripheral portion of the bottom surface being outside a periphery of the chip, and the central portion of the bottom surface being within and outside the periphery of the chip.

Regarding claims 25 and 35, Nakamura et al. discloses in Fig. 1, column 6, lines 49 ~ 55 and column 8, lines 53 ~ 58 the first single-piece housing portion being a transfer molded material, and the second single-piece housing portion being not a transfer molded material. Further, the limitation "transfer molded material" is a product-by-process claim language. Even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re

Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90** (**209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 26, Nakamura et al. discloses in Fig. 1 the peripheral portion of the bottom surface protruding a first distance below the central portion of the bottom surface, the terminal protruding a second distance below the central portion of the bottom surface, and the first distance being greater than the second distance.

Regarding claim 27, Nakamura et al. discloses in Fig. 1 and Fig. 4 the peripheral portion of the bottom surface being shaped as a rectangular peripheral ledge.

Regarding claim 28, Shin et al. discloses in Fig. 1A, Fig. 1B and Fig. 10B the terminal being within a periphery of the chip, and the lead being outside the periphery of the chip.

Regarding claim 29, Shin et al. discloses in Fig. 1A, Fig. 10B and Fig. 14 the device including a plurality of terminals and leads, the chip including a plurality of pads, each of the terminals are electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through the side surface and an opposing peripheral side surface of the insulative housing.

Regarding claims 30 and 40, Shin et al. discloses in Fig. 1A, Fig. 1B and Fig. 10B the device being devoid of wire bonds, TAB leads and solder joints.

Regarding claim 31, Shin et al. discloses in Fig. 1A, Fig. 1B, Fig. 10B, Fig. 14 and column 6, lines 36 ~ 40 a semiconductor package device, comprising:

- an insulative housing (40) with a top surface, a bottom surface, and four peripheral side surfaces between the top and bottom surfaces;
- a semiconductor chip (20) within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, and the upper surface includes a conductive pad, the upper surface faces towards the bottom surface and faces away from the top surface, and the insulative housing contacts the lower surface;
- a terminal (4 and 4') that protrudes downwardly from and extends through a central portion of the bottom surface and is spaced from the side surfaces and is electrically connected to the pad; and
- a lead (2) that protrudes laterally from and extends through one of the side surfaces and is electrically connected to the pad,
- wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

Shin et al. does not disclose the bottom surface including a peripheral portion shaped as a rectangular peripheral ledge adjacent to the side surfaces and a recessed central portion within the peripheral portion and spaced from the side surfaces, and the peripheral portion protrudes downwardly from the central portion and extends a first

distance below the central portion and wherein the terminal extends a second distance below the central portion, and the first distance is greater than the second distance. However, Nakamura et al. discloses in Fig. 1 and Fig. 4 a bottom surface (A) including a peripheral portion (B) shaped as a rectangular peripheral ledge adjacent to the side surfaces and a recessed central portion (area of 8) within the peripheral portion and spaced from the side surfaces, and the peripheral portion protrudes downwardly from the central portion and extends a first distance below the central portion and wherein a terminal (4) extends a second distance below the central portion, and the first distance is greater than the second distance. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Shin et al. by using the peripheral portion as taught by Nakamura et al. The ordinary artisan would have been motivated to modify Shin et al. in the manner described above for at least the purpose of providing a firm electrical connection with a circuit conductor layer formed on a substrate in a semiconductor device (column 5, lines 55 ~ 57).

Regarding claim 36, Nakamura et al. discloses in Fig. 1 the first distance being about twice the second distance.

Regarding claim 37, Nakamura et al. discloses in Fig. 1 the peripheral portion of the bottom surface being integral with the side surfaces and non-integral with the central portion of the bottom surface.

Regarding claim 38, Shin et al. discloses in Fig. 10B the terminal being within a periphery of the chip, and the peripheral portion of the bottom surface is outside the periphery of the chip.

Regarding claim 39, Shin et al. discloses in Fig. 1A, Fig. 10B and Fig. 14 the device including a plurality of terminals and leads, the chip including a plurality of pads, each of the terminals being electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the central portion of the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through two of the side surfaces that oppose one another.

7. Claims 41, 45 ~ 51, 57 ~ 60, 101, 105 ~ 111 and 117 ~ 120 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin et al. in view of Huang et al.

Regarding claim 41, Shin et al. discloses in Fig. 1A, Fig. 1B, Fig. 10B, Fig. 14 and column 6, lines 36 ~ 40 a semiconductor package device, comprising:

- an insulative housing (40) with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces;
- a semiconductor chip (20) within the insulative housing, wherein the chip includes an upper surface and a lower surface, and the upper surface includes a conductive pad;
- a terminal (4) that protrudes downwardly from and extends through the bottom surface and is electrically connected to the pad; and
- a lead (2) that protrudes laterally from and extends through the side surface and is electrically connected to the pad,

- wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

Shin et al. does not disclose the lead includes a recessed portion. However, Huang et al. discloses in Fig. 3 a lead (202) including a recessed portion (226) that contacts and extends into an insulative housing (218) and is spaced from top and bottom surfaces and does not overlap a chip (208) and a non-recessed portion (an area of 206b) that contacts and extends outside the insulative housing (218) and is adjacent to the recessed portion and the bottom surface. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Shin et al. by using the peripheral portion as taught by Huang et al. The ordinary artisan would have been motivated to modify Shin et al. in the manner described above for at least the purpose of increasing the encapsulating area of the molding compound on the surface of the lead (column 4, lines 20 ~ 24).

Regarding claims 45 and 105, Shin et al. discloses in Fig. 1A, Fig. 1B and Fig. 10B the terminal being the only electrical conductor that extends through the top or bottom surfaces and being electrically connected to the pad.

Regarding claim 46, Shin et al. discloses in Fig. 1A, Fig. 1B and Fig. 10B the terminal being a plated metal. Further, the limitation "plated metal" is a product-by-process claim language. Even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the

claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claims 47 and 106, Shin et al. discloses in Fig. 1A, Fig. 1B and Fig. 10B the terminal being within a periphery of the chip, and the lead being outside the periphery of the chip.

Regarding claims 48 and 108, Shin et al. discloses in Fig. 1A, Fig. 1B and Fig. 10B the device being devoid of an electrical conductor that extends through the top surface and being electrically connected to the pad.

Regarding claims 49 and 109, Shin et al. discloses in Fig. 1A, Fig. 10B and Fig. 14 the device including a plurality of terminals and leads, the chip including a plurality of pads, each of the terminals being electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through the side surface and an opposing peripheral side surface of the insulative housing.

Regarding claims 50, 60, 110 and 120, Shin et al. discloses in Fig. 1A, Fig. 1B and Fig. 10B the device being devoid of wire bonds, TAB leads and solder joints.

Regarding claim 51, Shin et al. discloses in Fig. 1A, Fig. 1B, Fig. 10B, Fig. 14 and column 6, lines 36 ~ 40 A semiconductor package device, comprising:

- an insulative housing (40) with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces;
- a semiconductor chip (20) within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, the upper surface includes a conductive pad (31), the upper surfaces faces towards the bottom surface and faces away from the top surface, and the insulative housing contacts the lower surface;
- a terminal (4 and 4') that protrudes downwardly from and extends through the bottom surface and is spaced from the side surface and is electrically connected to the pad; and
- a lead (2) that protrudes laterally from and extends through the side surface and is electrically connected to the pad,
- wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

Shin et al. does not disclose the lead includes a recessed portion. However, Huang et al. discloses in Fig. 3 a lead (202) including a recessed portion (226) that contacts and extends into an insulative housing (218) and is spaced from top and bottom surfaces and does not overlap a chip (208) and a non-recessed portion (an area of 206b) that contacts

and extends outside the insulative housing (218) and is adjacent to the recessed portion and the bottom surface. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Shin et al. by using the peripheral portion as taught by Huang et al. The ordinary artisan would have been motivated to modify Shin et al. in the manner described above for at least the purpose of increasing the encapsulating area of the molding compound on the surface of the lead (column 4, lines 20 ~ 24).

Regarding claims 57 and 117, Shin et al. discloses in Fig. 1A, Fig. 1B and Fig. 10B the terminal being within a periphery of the chip and outside a periphery of the pad, and the lead being outside the periphery of the chip.

Regarding claim 58, Shin et al. discloses in Fig. 10B and column 21, lines 22 ~ 28 the terminal being integral with a routing line that is plated on the lead inside the insulative housing, outside a periphery of the terminal and outside a periphery of the chip. Further, the limitation "plated on the lead" is a product-by-process claim language. Even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does

not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claims 59 and 119, Shin et al. discloses in Fig. 1A, Fig. 1B and Fig. 10B the device including a plurality of terminals and leads, the chip including a plurality of pads, each of the terminals being electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through the side surface and an opposing peripheral side surface of the insulative housing.

Regarding claim 101, Shin et al. discloses in Fig. 1A, Fig. 1B, Fig. 10B, Fig. 14 and column 6, lines 36 ~ 40 a semiconductor package device, comprising:

- an insulative housing (40) with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces;
- a semiconductor chip (20) within the insulative housing, wherein the chip includes an upper surface and a lower surface, and the upper surface includes a conductive pad;
- a terminal (4) that protrudes downwardly from and extends through the bottom surface and is electrically connected to the pad; and
- a lead (2) that protrudes laterally from and extends through the side surface and is electrically connected to the pad,

- wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

Shin et al. does not disclose the lead includes a recessed portion. However, Huang et al. discloses in Fig. 3 a lead (202) including a recessed portion (226) that extends into the insulative housing (218) and is spaced from top and bottom surfaces and a non-recessed portion (an area of 206b) that extends outside the insulative housing (218) and is adjacent to the recessed portion and contacts the insulative housing, the recessed and non-recessed portions each include four outer surfaces, three of the outer surfaces of the recessed and non-recessed portions that do not face in the same direction as the bottom surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, one of the outer surfaces of the recessed and non-recessed portions that face in the same direction as the bottom surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Shin et al. by using the peripheral portion as taught by Huang et al. The ordinary artisan would have been motivated to modify Shin et al. in the manner described above for at least the purpose of increasing the encapsulating area of the molding compound on the surface of the lead (column 4, lines 20 ~ 24).

Regarding claims 107 and 118, Shin et al., as modified, discloses the terminal being integral with a planar routing line that overlaps the lead and the pad and contacts the lead inside the insulative housing, outside a periphery of the terminal and outside a periphery of the chip.

Regarding claim 111, Shin et al. discloses in Fig. 1A, Fig. 1B, Fig. 10B, Fig. 14 and column 6, lines 36 ~ 40 a semiconductor package device, comprising:

- an insulative housing (40) with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces;
- a semiconductor chip (20) within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, and the upper surface includes a conductive pad, the upper surface faces towards the bottom surface and faces away from the top surface, and the insulative housing contacts the lower surface;
- a terminal (4) that protrudes downwardly from and extends through the bottom surface and is spaced from the side surface and is electrically connected to the pad; and
- a lead (2) that protrudes laterally from and extends through the side surface and is electrically connected to the pad,
- wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

Shin et al. does not disclose the lead includes a recessed portion. However, Huang et al. discloses in Fig. 3 a lead (202) including a recessed portion (226) that extends into the insulative housing (218) and is spaced from top and bottom surfaces and a non-recessed portion (an area of 206b) that extends outside the insulative housing (218) and is adjacent to the recessed portion and contacts the insulative housing, the recessed and non-recessed portions each include four outer surfaces, three of the outer surfaces of the

recessed and non-recessed portions that do not face in the same direction as the bottom surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, one of the outer surfaces of the recessed and non-recessed portions that face in the same direction as the bottom surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Shin et al. by using the peripheral portion as taught by Huang et al. The ordinary artisan would have been motivated to modify Shin et al. in the manner described above for at least the purpose of increasing the encapsulating area of the molding compound on the surface of the lead (column 4, lines 20 ~ 24).

8. Claims 42 ~ 44, 52 ~ 56, 102 ~ 104 and 112 ~ 116 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin et al. and Huang et al. as applied to claims 41, 51 and 101 above, and further in view of Nakamura et al.

Regarding claims 42 and 102, Shin et al., as modified, discloses the claimed invention except for the insulative housing including a first single-piece housing portion that contacts the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion and the terminal. However, Nakamura et al. discloses in Fig. 1 an insulative housing (7 and 8) including a first single-piece housing portion (7) that contacts a lead (2) and is spaced from a terminal (4) and a second single-piece housing portion (8) that contacts the first single-piece housing portion and the terminal. Thus, it would have been obvious to one of ordinary skill in the

art at the time when the invention was made to further modify Shin et al. by using the first and second single-piece housing portion for the insulative housing as taught by Nakamura et al. The ordinary artisan would have been motivated to further modify Shin et al. in the manner described above for at least the purpose of providing a firm electrical connection with a circuit conductor layer formed on a substrate in a semiconductor device (column 5, lines 55 ~ 57).

Regarding claims 43 and 103, Nakamura et al. discloses in Fig. 1 the first single-piece housing portion contacting the lower surface.

Regarding claims 44 and 104, Nakamura et al. discloses in Fig. 1 the insulative housing consisting of the first and second single-piece housing portions.

Regarding claims 52 and 112, Shin et al., as modified, discloses the claimed invention except for the insulative housing consists of a first single-piece housing portion that contacts the lower surface and the lead and is spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion and the terminal. However, Nakamura et al. discloses in Fig. 1 an insulative housing (7 and 8) consisting of a first single-piece housing portion (7) that contacts a lower surface and a lead (2) and is spaced from a terminal (4) and a second single-piece housing portion (8) that contacts the first single-piece housing portion and the terminal. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Shin et al. by using the first and second single-piece housing portion for the insulative housing as taught by Nakamura et al. The ordinary artisan would have been motivated to further modify Shin et al. in the manner described above for at least the

purpose of providing a firm electrical connection with a circuit conductor layer formed on a substrate in a semiconductor device (column 5, lines 55 ~ 57).

Regarding claims 53 and 113, Nakamura et al. discloses in Fig. 1 the first single-piece housing portion providing the top surface, the side surface and a peripheral portion of the bottom surface, and the second single-piece housing portion providing a central portion of the bottom surface within the peripheral portion of the bottom surface.

Regarding claims 54 and 114, Nakamura et al. discloses in Fig. 1 the peripheral portion of the bottom surface being outside a periphery of the chip, and the central portion of the bottom surface being within and outside the periphery of the chip.

Regarding claims 55 and 115, Nakamura et al. discloses in Fig. 1 the first single-piece housing portion being a transfer molded material, and the second single-piece housing portion being not a transfer molded material. Further, the limitation "transfer molded material" is a product-by-process claim language. Even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must

be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claims 56 and 116, Nakamura et al. discloses in Fig. 1 the second single-piece housing portion including first and second opposing surfaces, the first surface contacting the lead and the second surface providing a portion of the bottom surface.

9. Claims 61, 65, 66, 68, 69, 70, 71, 78, 79 and 80 are rejected under 35 U.S.C. 103(a) as being unpatentable over Osawa in view of McShane et al.

Regarding claim 61, Osawa discloses in Fig. 1 a semiconductor package device, comprising:

- an insulative housing (7) with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces;
- a semiconductor chip (1) within the insulative housing, wherein the chip includes an upper surface and a lower surface, and the upper surface includes a conductive pad (2);
- a routing line (4) within the insulative housing that overlaps and is electrically connected to the pad;
- a terminal (an area of 4 which connected to an element 5) that protrudes downwardly from and is integral with the routing line, protrudes downwardly

from and extends through the bottom surface and is electrically connected to the pad; and

- a lead (6) that contacts and is not integral with the routing line, protrudes laterally from and extends through the side surface and is electrically connected to the pad, wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another by the routing line inside the insulative housing and outside the chip.

Osawa does not disclose the lead that protrudes downward. However, McShane et al. teaches in Fig. 2 a lead (48) that protrudes downward. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Osawa by using the lead to protrude downward as taught by McShane et al. The ordinary artisan would have been motivated to modify Osawa in the manner described above for at least the purpose of providing a flexibility in substrate mounting (column 4, lines 50 ~ 51).

Regarding claim 65, Osawa discloses in Fig. 1 the terminal being the only electrical conductor that extends through the top or bottom surfaces and being electrically connected to the pad.

Regarding claim 66, Osawa discloses in Fig. 1 the routing line and the terminal being a plated metal. Further, the limitation "plated metal" is a product-by-process claim language. Even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-

process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 68, Osawa, as modified, discloses the device being devoid of an electrical conductor that extends through the top surface and is electrically connected to the pad.

Regarding claim 69, Osawa discloses in Fig. 1 the device including a plurality of terminals and leads, the chip including a plurality of pads, each of the terminals being electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through the side surface and an opposing peripheral side surface of the insulative housing.

Regarding claims 70 and 80, Osawa discloses in Fig. 1 the device being devoid of wire bonds, TAB leads and solder joints.

Regarding claim 71, Osawa discloses in Fig. 1 a semiconductor package device, comprising:

- an insulative housing (7) with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces;
- a semiconductor chip (1) within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, the upper surface includes a conductive pad (2), the upper surface faces towards the bottom surface and faces away from the top surface, and the insulative housing contacts the lower surface;
- a routing line (4) within and surrounded by the insulative housing, wherein the routing line overlaps and is electrically connected to the pad;
- a terminal (an area of 4 which connected to an element 5) that protrudes downwardly from and is integral with the routing line, protrudes downwardly from and extends through the bottom surface, is spaced from the side surface and is electrically connected to the pad; and
- a lead (6) that contacts and is not integral with the routing line, protrudes laterally from and extends through the side surface and is electrically connected to the pad, wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another inside the insulative housing and outside the chip.

Osawa does not disclose the lead that protrudes downward. However, McShane et al. discloses in Fig. 2 a lead (48) that protrudes downward. Thus, it would have been

obvious to one of ordinary skill in the art at the time when the invention was made to modify Osawa by using the lead to protrude downward as taught by McShane et al. The ordinary artisan would have been motivated to modify Osawa in the manner described above for at least the purpose of providing a flexibility in substrate mounting (column 4, lines 50 ~ 51).

Regarding claim 78, Osawa discloses in Fig. 1 the routing line being plated on the lead inside the insulative housing, outside a periphery of the terminal and outside a periphery of the chip. Further, the limitation "plated on the lead" is a product-by-process claim language. Even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 79, Osawa discloses in Fig. 1 the device including a plurality of terminals and leads, the chip including a plurality of pads, each of the terminals being electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through the side surface and an opposing peripheral side surface of the insulative housing.

10. Claims 62 ~ 64, 72 ~ 76, 81 ~ 87, 89 ~ 97, 99 and 100 are rejected under 35 U.S.C. 103(a) as being unpatentable over Osawa and McShane et al. as applied to claims 61 and 71 above, and further in view of Happ.

Regarding claim 62, Osawa, as modified, discloses the claimed invention except for the insulative housing including a first single-piece housing portion that contacts the routing line and the lead and being spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion, the routing line and the terminal. However, Happ discloses in Fig. 7, Fig. 8 and column 9, lines 16 ~ 39 an insulative housing (140 and 142) including a first single-piece housing portion (140) that contacts a routing line (86) and a lead (82) and being spaced from a terminal (100) and a second single-piece housing portion (142) that contacts the first single-piece housing portion, the routing line and the terminal. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Osawa by using the first and second single-piece housing portion for the insulative housing as taught by Happ. The ordinary artisan would have been motivated to further modify

Osawa in the manner described above for at least the purpose of adding further mechanical strength and rigidity to the overall structure (column 9, lines 24 ~ 25).

Regarding claim 63, Happ discloses in Fig. 7, Fig. 8 and column 9, lines 32 ~ 39 the first single-piece housing portion contacting the lower surface.

Regarding claim 64, Happ discloses in Fig. 7, Fig. 8 and column 9, lines 32 ~ 39 the insulative housing consisting of the first and second single-piece housing portions.

Regarding claim 72, Osawa, as modified, discloses the claimed invention except for the insulative housing consisting of a first single-piece housing portion that contacts the lower surface, the routing line and the lead and being spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion, the routing line and the terminal. However, Happ discloses in Fig. 7, Fig. 8 and column 9, lines 16 ~ 39 an insulative housing (140 and 142) consisting of a first single-piece housing portion (140) that contacts a lower surface, a routing line (86) and a lead (82) and being spaced from a terminal (100) and a second single-piece housing portion (142) that contacts the first single-piece housing portion, the routing line and the terminal. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Osawa by using the first and second single-piece housing portion for the insulative housing as taught by Happ. The ordinary artisan would have been motivated to further modify Osawa in the manner described above for at least the purpose of adding further mechanical strength and rigidity to the overall structure (column 9, lines 24 ~ 25).

Regarding claim 73, Happ discloses in Fig. 7, Fig. 8 and column 9, lines 32 ~ 39 the first single-piece housing portion providing the top surface, the side surface and a

peripheral portion of the bottom surface, and the second single-piece housing portion providing a central portion of the bottom surface within the peripheral portion of the bottom surface.

Regarding claim 74, Happ discloses in Fig. 7, Fig. 8 and column 9, lines 32 ~ 39 the peripheral portion of the bottom surface being outside a periphery of the chip, and the central portion of the bottom surface being within and outside the periphery of the chip.

Regarding claim 75, Happ discloses in Fig. 7, Fig. 8 and column 9, lines 32 ~ 39 the first single-piece housing portion being a transfer molded material, and the second single-piece housing portion being not a transfer molded material. Further, the limitation "transfer molded material" is a product-by-process claim language. Even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not.

Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 76, Happ discloses in Fig. 7, Fig. 8 and column 9, lines 32 ~ 39 the second single-piece housing portion including first and second opposing surfaces, the first surface contacting the routing line and the second surface providing a portion of the bottom surface.

Regarding claim 81, Osawa discloses in Fig. 1 a semiconductor package device, comprising:

- an insulative housing (7) with a top surface, a bottom surface, and a peripheral side surface between the top and bottom surfaces;
- a semiconductor chip (1) within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, the upper surface includes a conductive pad (2);
- a routing line (4) within and surrounded by the insulative housing, wherein the routing line overlaps and is electrically connected to the pad;
- a terminal (an area of 4 which connected to an element 5) that protrudes downwardly from and is integral with the routing line, protrudes downwardly from and extends through the central portion of the bottom surface, is spaced from the side surface and is electrically connected to the pad; and
- a lead (6) that contacts and is not integral with the routing line, protrudes laterally from and extends through one of the side surfaces and is electrically connected to the pad, wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal

and the lead are electrically connected to one another by the routing line inside the insulative housing and outside the chip.

Osawa does not disclose the lead that protrudes downward. However, McShane et al. discloses in Fig. 2 a lead (48) that protrudes downward. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Osawa by using the lead to protrude downward as taught by McShane et al. The ordinary artisan would have been motivated to modify Osawa in the manner described above for at least the purpose of providing a flexibility in substrate mounting (column 4, lines 50 ~ 51).

Further, Osawa does not disclose the bottom surface including a peripheral portion adjacent to the side surfaces and a central portion within the peripheral portion and spaced from the side surfaces, and the peripheral portion protrudes downwardly from the central portion. However, Happ discloses in Fig. 5 a bottom surface of an insulative housing (112) including a peripheral portion (at the side wall of 113) adjacent to side surfaces and a central portion (113) within the peripheral portion and spaced from the side surfaces, and the peripheral portion protrudes downwardly from the central portion. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Osawa by using the peripheral portion to protrude downwardly from the central portion as taught by Happ. The ordinary artisan would have been motivated to further modify Osawa in the manner described above for at least the purpose of enhancing the heat dissipation properties of the unit (column 7, lines 73 ~ 75).

Regarding claims 82 and 92, Osawa, as modified, discloses the claimed invention except for the insulative housing consisting of a first single-piece housing portion that

contacts the lower surface, the routing line and the lead and being spaced from the terminal and a second single-piece housing portion that contacts the first single-piece housing portion, the routing line and the terminal. However, Happ discloses in Fig. 7, Fig. 8 and column 9, lines 16 ~ 39 an insulative housing (140 and 142) consisting of a first single-piece housing portion (140) that contacts the lower surface, a routing line (86) and a lead (82) and being spaced from a terminal (100) and a second single-piece housing portion (142) that contacts the first single-piece housing portion, the routing line and the terminal. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Osawa by using the first and second single-piece housing portion for the insulative housing as taught by Happ. The ordinary artisan would have been motivated to further modify Osawa in the manner described above for at least the purpose of adding further mechanical strength and rigidity to the overall structure (column 9, lines 24 ~ 25).

Regarding claims 83 and 93, Happ discloses in Fig. 7, Fig. 8 and column 9, lines 32 ~ 39 the first single-piece housing portion providing the top surface, the side surfaces and the peripheral portion of the bottom surface, and the second single-piece housing portion providing the central portion of the bottom surface.

Regarding claims 84 and 94, Happ discloses in Fig. 7, Fig. 8 and column 9, lines 32 ~ 39 the peripheral portion of the bottom surface being outside a periphery of the chip, and the central portion of the bottom surface being within and outside the periphery of the chip.

Regarding claims 85 and 95, Happ discloses in Fig. 7, Fig. 8 and column 9, lines 32 ~ 39 the first single-piece housing portion being a transfer molded material, and the

second single-piece housing portion being not a transfer molded material. Further, the limitation "transfer molded material" is a product-by-process claim language. Even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 86, Osawa, as modified, discloses the peripheral portion of the bottom surface protruding a first distance below the central portion of the bottom surface, the terminal protruding a second distance below the central portion of the bottom surface, and the first distance being greater than the second distance.

Regarding claim 87, Happ discloses in Fig. 5 the peripheral portion of the bottom surface being shaped as a rectangular peripheral ledge.

Regarding claims 89 and 99, Osawa discloses in Fig. 1 the device including a plurality of terminals and leads, the chip including a plurality of pads, each of the terminals being electrically connected to one of the leads and one of the pads inside the insulative housing and outside the chip, the terminals are arranged as an array that protrudes downwardly from and extends through the central portion of the bottom surface, and the leads are arranged as TSOP leads that protrude laterally from and extend through two of the side surfaces that oppose one another.

Regarding claims 90 and 100, Osawa discloses in Fig. 1 the device being devoid of wire bonds, TAB leads and solder joints.

Regarding claim 91, Osawa discloses in Fig. 1 a semiconductor package device, comprising:

- an insulative housing (7) with a top surface, a bottom surface, and four peripheral side surfaces between the top and bottom surfaces;
- a semiconductor chip (1) within and surrounded by the insulative housing, wherein the chip includes an upper surface and a lower surface, the upper surface includes a conductive pad (2), the upper surface faces towards the bottom surface and faces away from the top surface, and the insulative housing contacts the lower surface;
- a routing line (4) within and surrounded by the insulative housing, wherein the routing line overlaps and is electrically connected to the pad;
- a terminal (an area of 4 which connected to an element 5) that protrudes downwardly from and is integral with the routing line, protrudes downwardly from and extends through the central portion of the bottom surface, is spaced

from the side surface and is electrically connected to the pad, wherein the terminal extends a second distance below the central portion, and the first distance is greater than the second distance; and

- a lead (6) that contacts and is not integral with the routing line, protrudes laterally from and extends through one of the side surfaces and is electrically connected to the pad, wherein the terminal and the lead are spaced and separated from one another outside the insulative housing, and the terminal and the lead are electrically connected to one another by the routing line inside the insulative housing and outside the chip.

Osawa does not disclose the lead that protrudes downward. However, McShane et al. discloses in Fig. 2 a lead (48) that protrudes downward. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Osawa by using the lead to protrude downward as taught by McShane et al. The ordinary artisan would have been motivated to modify Osawa in the manner described above for at least the purpose of providing a flexibility in substrate mounting (column 4, lines 50 ~ 51).

Further, Osawa does not disclose the bottom surface including a peripheral portion shaped as a rectangular peripheral ledge adjacent to the side surfaces and a recessed central portion within the peripheral portion and spaced from the side surfaces, and the peripheral portion protrudes downwardly from the central portion and extends a first distance below the central portion. However, Happ discloses in Fig. 5 a bottom surface of an insulative housing (112) including a peripheral portion (at the side wall of 113) shaped as a rectangular peripheral ledge adjacent to side surfaces and a recessed

central portion (113) within the peripheral portion and spaced from the side surfaces, and the peripheral portion protrudes downwardly from the central portion and extends a first distance below the central portion. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Osawa by using the peripheral portion to protrude downwardly from the central portion as taught by Happ. The ordinary artisan would have been motivated to further modify Osawa in the manner described above for at least the purpose of enhancing the heat dissipation properties of the unit (column 7, lines 73 ~ 75).

Regarding claim 96, Osawa, as modified, discloses the first distance being about twice the second distance.

Regarding claim 97, Osawa, as modified, discloses the peripheral portion of the bottom surface being integral with the side surfaces and non-integral with the central portion of the bottom surface.

11. Claims 67 and 77 are rejected under 35 U.S.C. 103(a) as being unpatentable over Osawa and McShane et al. as applied to claims 61 and 71 above, and further in view of Kimura.

Regarding claims 67 and 77, Osawa discloses in Fig. 1 the terminal being outside a periphery of the pad, the routing line being within and outside the periphery of the chip, and the lead being outside the periphery of the chip. Osawa does not disclose the terminal being within a periphery of the chip. However, Kimura discloses in Fig. 4E a terminal (an exposed are of 5B from a resin 7) being within a periphery of a chip (1). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was

made to further modify Osawa by using the terminal to be within a periphery of the chip as taught by Kimura. The ordinary artisan would have been motivated to further modify Osawa in the manner described above for at least the purpose of increasing speed of I/O signals.

12. Claims 88 and 98 are rejected under 35 U.S.C. 103(a) as being unpatentable over Osawa, Happ and McShane et al. as applied to claims 81 and 91 above, and further in view of Kimura.

Regarding claims 88 and 98, Osawa discloses in Fig. 1 the terminal being outside a periphery of the pad, the routing line being within and outside the periphery of the chip, and the lead being outside the periphery of the chip, and the peripheral portion of the bottom surface being outside the periphery of the chip. Osawa does not disclose the terminal being within a periphery of the chip. However, Kimura discloses in Fig. 4E a terminal (an exposed are of 5B from a resin 7) being within a periphery of a chip (1). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Osawa by using the terminal to be within a periphery of the chip as taught by Kimura. The ordinary artisan would have been motivated to further modify Osawa in the manner described above for at least the purpose of increasing speed of I/O signals.

Response to Arguments

13. Applicant's arguments filed on May 8, 2003 have been fully considered but they are not persuasive.

On page 36, applicant argues "claim 10 recites 'the device is devoid of wire bonds, TAB leads and solder joints.' Claim 20 recites similar limitations. Shin et al. fails to teach or suggest this approach ... Fig. 10B discloses lead 2 electrically connected to chip 20 by solder joint 31" This argument is not persuasive. Shin et al. discloses in column 16, line 43 the element 31 being a bump. Thus, Shin et al. meets the limitations in claims 10 and 20.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). Contrary to applicant's assertion and as stated in previous rejection which is mailed on April 23, 2003, motivation was established by Nakamura et al., specifically in column 5, lines 55 ~ 57 (to provide a firm electrical connection with a circuit conductor layer formed on a substrate in a semiconductor device).

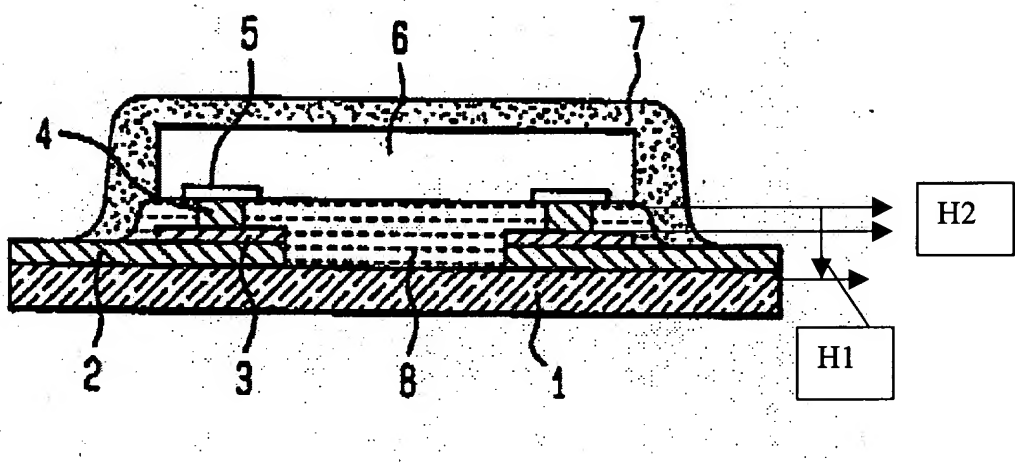
Further, applicant's argument against Nakamura et al. have been fully considered but not deemed to be persuasive because only teaching the Examiner being relied on therefrom is first and second single-piece housing portions for the insulative housing as defined in amended claims 1 and 11. Therefore, arguments thereagainst are not deemed to be relevant to how Nakamura et al. is being applied in the rejection.

Furthermore, applicant argues "claim 21 recites that the peripheral portion protrudes downwardly from a central portion. In *Nakamura et al.,* resin coating 7 does not protrude downwardly from resin layer 8. Instead, resin coating 7 and resin layer 8 are bounded by light-transmitting substrate 1." This argument is not persuasive. Since applicant does not specifically defined the beginning point of the protrusion (e.g. with respect to which surface, upper or bottom surface of central portion, etc.), upper surface of Nakamura et al.'s central portion shows that the peripheral portion protrudes downwardly from the upper surface of the central portion. Therefore, a combined structure of Shin et al. and Nakamura et al. meets the rejected claim.

Finally, applicant argues "claim 31 also recites that peripheral portion extends a first distance below the central portion, the terminal extends a second distance below the central portion, and the first distance is greater than the second distance." Such argument is not persuasive because claim 31, lines 4 and 5 clearly defined that the central portion is a recessed central portion. Since the central portion is a recessed central portion, the bottom surface of the central portion is the lower surface of the chip. Thus, Nakamura et

al. clearly shows in Fig. 1 that the first distance (H1) is greater than the second distance (H2).

FIG. 1



For the above reasons, the rejection is maintained.

Conclusion

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7382 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
August 7, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800